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High mobility organic transistor patterned by the shadow-mask with all structure on a plastic substrate

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Abstract Pentacene thin film transistors fabricated without photolithographic patterning were fabricated on the plastic substrates. Both the organic/inorganic thin films and metallic electrode were patterned by shifting the position of the shadow-mask which accompanies the substrate throughout the deposition process. By using an optically transparent zirconium oxide (ZrO_2) as a gate insulator and octadecyltrimethoxysilane (OTMS) as an organic molecule for self-assembled monolayer (SAM) to increase the adhesion between the plastic substrate and gate insulator and the mobility with surface treatment, high-performance transistor with field effect mobility 0.66 cm^2/V s and $I_{on}/I_{off} > 10^5$ was formed on the plastic substrate. This technique will be applicable to all structure deposited at low temperature and suitable for an easy process for flexible display.

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Introduction

Organic thin films have been widely studied due to their potential for application related to large area, low-cost electronics and their compatibility with flexible substrate [1–4]. Significant improvements have been made in the performance of these materials through the optimization of deposition parameter, materials purification, and optimized design of device and gate geometry.

Among many organic materials, the mobility of pentacene was superior to that of the other organic candidate materials for Organic Thin Film Transistor (OTFT). It was also known that an undoped pentacene crystal is a p-type semiconductor. Also, it is usually deposited by thermal evaporation technique under specific process condition such as substrate and deposition rate [5]. However, processing of organic devices including pentacene is difficult. A typical problem in fabricating more advanced organic-based integrated circuits is that it is difficult to pattern the organic active layer using photolithography and etching, or to pattern layers deposited on top of the organic active layer. While bulk pentacene is relatively insoluble and non-reactive in the typical solvents used in photolithographic processing, Thin Film Transistor (TFT) performance is dramatically degraded after exposure to solvents [6].

In addition, the performance of the device on a plastic substrate is much lower than that of the device

on silicon and glass substrate. Most of all, the low thermal tolerance, poor surface morphology and non-rigidness of plastic substrate mainly account for the poor device performance [7].

In this study, we will present a technique for improving performance of an OTFT using the shadow-mask process. Shadow-mask is generally used to define the source/drain as an electrode and the pentacene as an active layer, but we expanded this technique to all layer of organic TFT with ZrO_2 as a gate dielectric layer, which is one of the most promising materials due to its high permittivity of 20–25, excellent adhesion and good mechanical stability with PES film [8, 9]. ZrO_2 is an attractive candidate since it has a high dielectric constant (15–22), a high breakdown field (15–20 MV/cm), a large band gap (5–7 eV) [10], and may be thermodynamically stable on silicon. Kinetically, however, interfacial reactions between ZrO_2 and silicon remain a critical issue in determining its applicability in MOS capacitors and MOSFETs. It has been used in waveguides and interferometers, and for coating high power laser mirrors [11, 12]. And, OTMS has been applied to improve the field effect mobility of OTFTs through the better quality of the organic active material/dielectric interface. The OTMS, which is well known as an important activator in the surface modification process, is one of the most widely used materials for the hydrophobic SAMs containing alkyl silanes, resulting in the chemical bond formation by an intermolecular interaction between OTMS and ZrO_2 [13]. We formed the OTMS on a hydrophilic ZrO_2 surface so that the long alkyl tails form a tightly packed monolayer while the Si adheres to the surface of ZrO_2 through Si–O covalent bonds [14, 15].

Experimental

In our process, OTFTs have been fabricated using evaporation chamber including optical aligner for shadow-mask process (Fig. 1a). This optical aligner located at top side on chamber to control through view port with the video-view split field microscope and the shadow-mask was designed for operation of aligns easy to evaporation process with align mark. Figure 1b shows a schematic diagram of the shadow-mask and substrate assembly. The substrate is held fixed while the mask can be moved in three different directions, namely X, Y and θ_z. The patterning of all layer is achieved by deposition through the four-level shadow-mask aperture, whose position relative to substrate is precisely aligned for etch layer.

Polyethersulfone (PES) films are used as flexible substrates. After curing of PES to eliminate the minute pin-holes for 60 min at 120 °C, Au of 80 nm thick as a gate electrode was thermally evaporated by using a shadow-mask under vacuum of less than 2×10^{-6} Torr. On the patterned gate electrode, a 250-nm thick ZrO_2 for gate dielectric layer was deposited by the e-beam at relatively low temperature (<120 °C). Following the

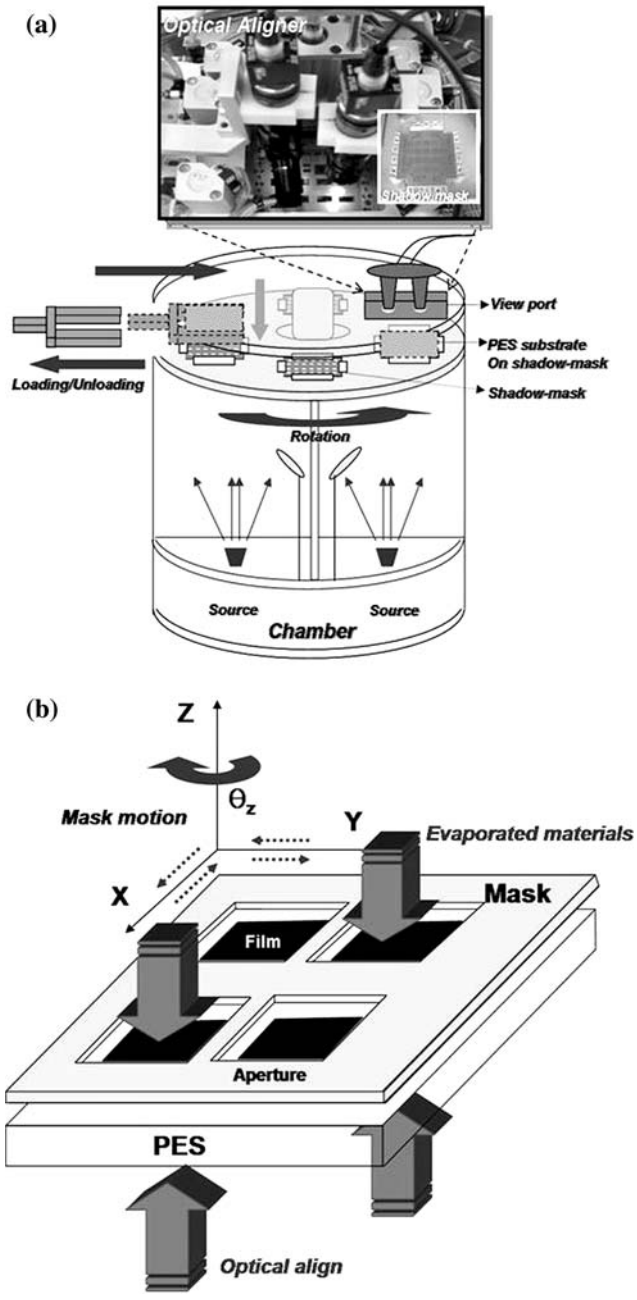

Fig. 1 A schematic diagram of evaporator including optical aligner for shadow-mask process. (**a**) Fundamental concept of shadow-mask process and (**b**) a schematic diagram of the shadow-mask and substrate assembly

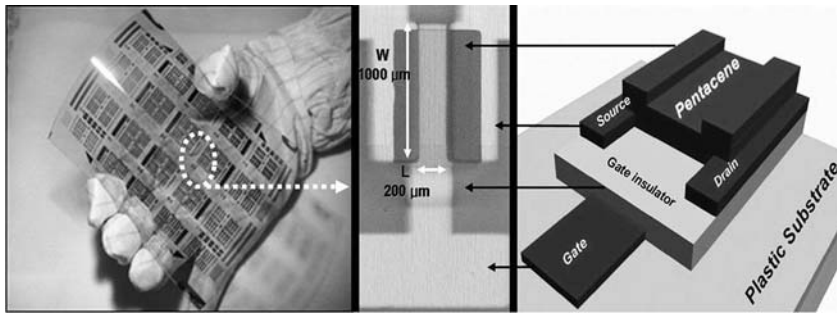

Fig. 2 Photograph of the fabricated pentacene TFT on plastic substrate and schematic structure of bottom-contact pentacene TFT

gate dielectric layer deposition, in order to have a good affinity of organic molecule on the surface of the dielectric layer, we modified the surface of ZrO_2 by using combinational SAMs of alkyl silanes. The SAMs deposition was performed by soaking a solution of OTMS/isopropanol (1:20/v:v) for 2–3 min under nitrogen atmosphere. Source and drain electrodes were aligned by the shadow-mask aligner consisting of 100 nm Au and were deposited onto the gate dielectric layer using thermal evaporation. The channel length L is 200 μm and width W is 1,000 μm.

Pentacene as an active layer was grown by vacuum evaporation at a working pressure of 2×10^{-6} Torr. During the pentacene deposition, the substrate temperature was held at 60 °C. The thickness of pentacene film was 100 nm with a deposition rate of 1 Å/s. A schematic diagram of bottom-contact structured OTFT used in this study and photograph of the fabricated device on flexible substrate were shown in Fig. 2.

Electrical measurements were performed at room temperature in air by using a parameter analyzer (HP4145, Hewlett-Packard). Capacitance measurements of the ZrO_2 were carried out by using a C–V analyzer (Keithly 590—1 MHz). The cross-sectional

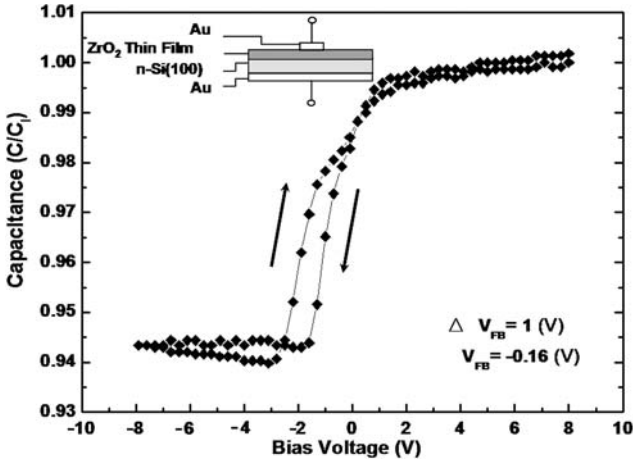

Fig. 3 High frequency (1 MHz) capacitance (C–V) characteristics of the dielectric layer (ZrO_2) deposited on a heavily doped n-type silicon substrate

structure was observed by scanning electron microscope (SEM). For the evidence of the reaction of the OTMS with ZrO_2, we took Infra-red spectroscopy with the reaction mixture. All the electrical measurements of fabricated devices were performed in a dark room without any considerations to prevent the degradation phenomena of pentacene film.

Results and discussion

Figure 3 presents the high frequency (1 MHz) capacitance–voltage (C–V) characteristics of Metal–Insulator–Silicon (MIS) structure in order to acquire the dielectric characteristics of ZrO_2. The capacitance was measured as the maximum value of 1 and the minimum value of 0.96 when the applied voltage was increased from –10 V to 10 V. The flat-band voltage of new oxide material was calculated as –0.16 V in the characteristic curve.

Figure 4 shows the cross-section image of the fabricated device of active area on PES substrate. The thickness of gate electrode (Au) was about 80 nm before ZrO_2 evaporation. The 250 nm thick ZrO_2 layer was evaporated on top of the gate electrode by e-beam evaporator. Finally, pentacene as an active layer was grown by vacuum evaporation at a working pressure of 2×10^{-6} Torr. The thickness of pentacene film was 100 nm with a deposition rate of 1 Å/s. During the formation of pentacene layer, the substrate temperature was held at 60 °C.

Figure 5 shows electrical characteristics of the organic pentacene TFTs with a channel width of 1,000 μm and length of 200 μm in the absence of the surface treatment. The kink phenomena shown in Fig. 5a drain current – drain voltage ($I_D - V_D$) characteristics are attributable to the increased surface potential barrier height between a pentacene organic layer and a gate dielectric layer, resulting in the serious device degradation. Figure 5b drain current – gate voltage ($I_D - V_G$) curve illustrates the electrical characteristics such as on/off current ratio of 10^4 and the

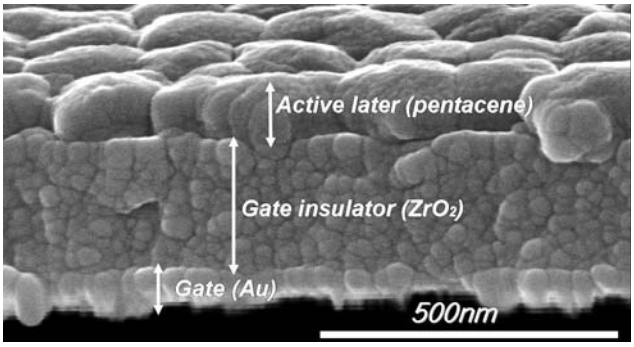

Fig. 4 SEM image of cross-sectional devices composed of PES/Au/ZrO_2/pentacene

field effect mobility of 0.12 cm^2/V s at the drain voltage of –0.1 V; all of these characteristics are similar to those commonly obtained for photo-lithographically defined pentacene TFTs.

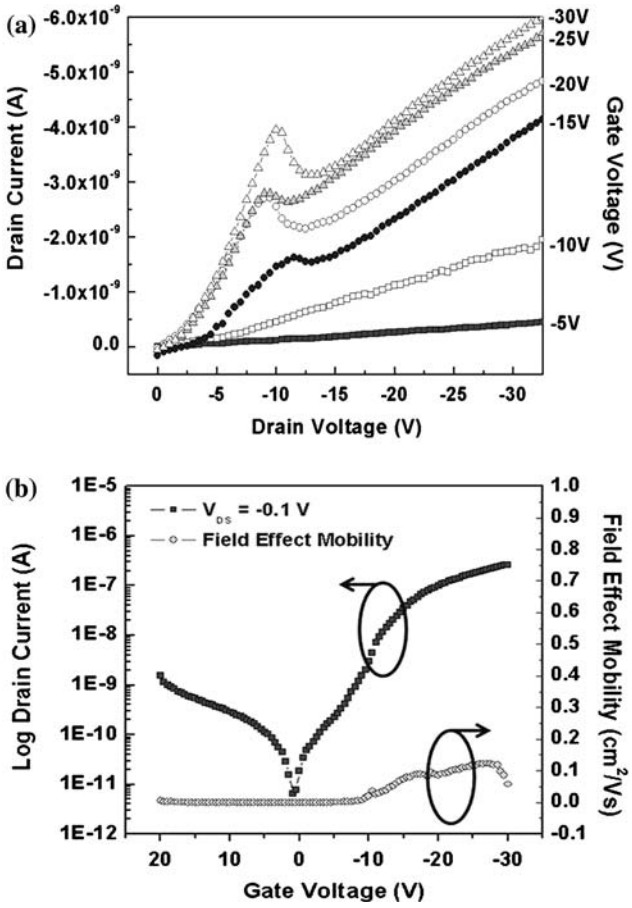

Fig. 5 Electrical properties of shadow-mask processed TFT in the absence of OTMS treatment on gate insulator. (**a**) Electrical characteristics of drain current (I_D) versus voltage (V_D) at various gate voltages (V_G) and (**b**) Electrical characteristics of I_D versus V_G and field effect mobility at drain voltages (V_D) of 0.1 V

However, considering the possible positive effect of the organic molecules modifying the surface of gate dielectrics, we applied OTMS as the organic molecules on the surface of gate dielectric layer. The OTMS deposited on the ZrO_2 surface was confirmed by Infra-red spectroscopy as shown in Fig. 6. Two sharp stretching bands at 2,921 cm^{-1} and 2,850 cm^{-1} indicates that the sample has an aliphatic C–H, which comes from the reacted OTMS (Fig. 6b). Two peaks at 1,459 cm^{-1} and 1,431 cm^{-1} are for the aliphatic C–H bending. In addition, one sharp stretching band at 1,083 cm^{-1} is for C–O single bond.

Figure 7(a) $I_D - V_D$ and (b) $I_D - V_G$ show electrical characteristics for the organic pentacene TFTs with a channel width of 1,000 μm and a channel length of 200 μm in the presence of the OTMS surface treatment on the gate dielectrics. It is clear that the organic pentacene TFTs with the OTMS treatment show the better device characteristics. The mobility increased up to 0.66 cm^2/V s and the on/off current ratio of 10^5 could be obtained. These remarkably improved characteristics of the OTFT seem to be ascribed to the

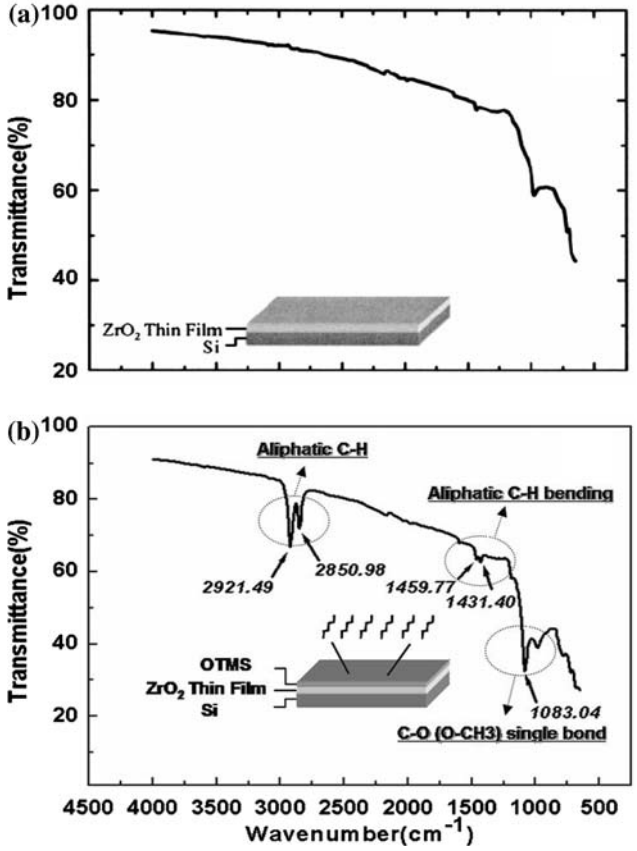

Fig. 6 Infra-red spectra of the ZrO_2–OTMS deposition. Sample was prepared by deposition of ZrO_2 on the silicon wafer followed by surface treatment of the OTMS

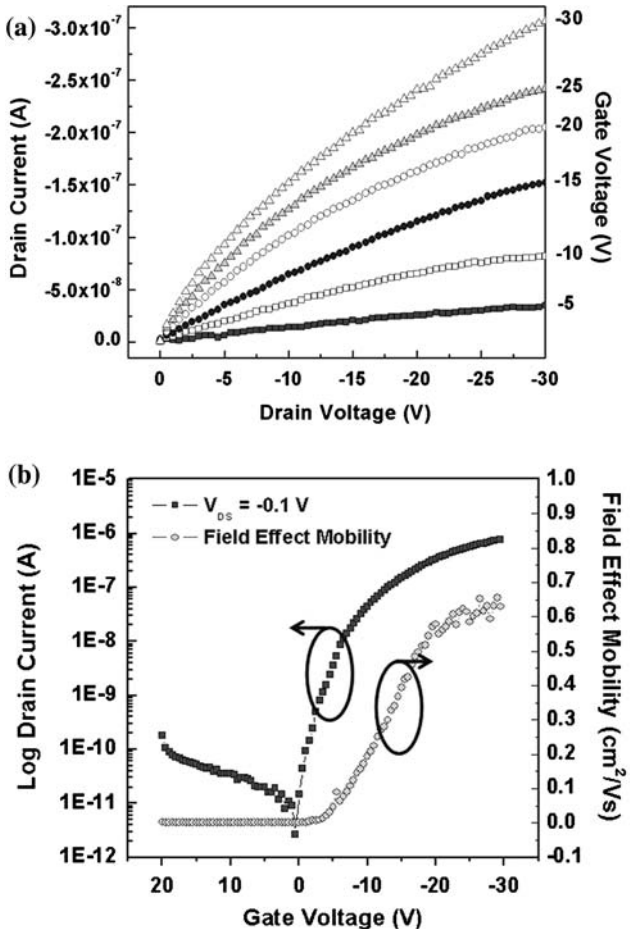

Fig. 7 Electrical properties of shadow-mask processed TFT in the presence of OTMS treatment on gate insulator. (**a**) Electrical characteristics of drain current (I_D) versus voltage (V_D) at various gate voltages (V_G) and (**b**) Electrical characteristics of I_D versus V_G and field effect mobility at drain voltages (V_D) of 0.1 V

uniformity of the pentacene grain as well as the enhanced contact edge effect between the surface modified gate dielectrics and organic pentacene molecules as mentioned earlier. In addition, the hydrophobic pentacene molecules became more feasible to bind with the hydrophobic tails of organic molecules on the surface treated gate dielectric layer. Therefore, we can understand that the intermolecular chemical reaction between the OTMS and ZrO_2 brings the more improved device performance. It can also be expected that a substitution reaction of the $-OCH_3$ group of the OTMS with the ZrO_2 gave a ZrO_2–OTMS compound on which the organic pentacene molecule was easily deposited because the van der Waal's lipophilic attraction between the OTMS and the pentacene are strong enough to have an intermolecular interaction, providing the excellent adhesion of the organic pentacene molecules on the dielectrics.

Conclusion

We have presented the electrical characteristics of pentacene organic thin film transistors fabricated on flexible polyethersulfone (PES) film through a four-level shadow-mask process. The alignment technique by using shadow-mask was used to form source/drain since it was expected to provide a low cost process and it is possible to one-step process from patterning to passivation without breaking vacuum in the chamber. Zirconium oxide as a new material layer, which has good properties as gate dielectric layer was used. It is found that chemical treatment of the gate dielectric surface with OTMS gives rise to a remarkable increase of field effect mobility 0.66 cm^2/V s and $I_{on}/I_{off} > 10^5$ formed on the plastic substrate. This technique will be applicable to all structure deposited at low temperature and suitable for an easy process for flexible display.

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